ABSTRACT

A 3 Dimensional EEPROM cell layout, process control, and device model means are proposed. This cell construct uses the pointing shapes of the intrinsic conducting electrodes, thin and high dielectric insulators to customize signal coupling capacitors between intrinsic terminals, and therefore to optimize cell efficiency and operating voltages. Array of the said cells are mixed with high density, low power Schottky-CMOS logic (SCL) gate arrays to implement various array operations. The invented memory-logic device possesses $4F^2$ area per storage unit with 4 multilevel charges, single contact space per logic fan-in or fan-out, and operates with 1.2V supply.

We have disclosed our invention with means and control schemes to obtain a compact cell. This cell has properties based on 3D geometrical details including film edge shapes, and composition of insulating materials in the intrinsic electrode constructs.